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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

Sheet

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of

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Complete if Known	
Application No.	10/749,912
Filing Date	December 30, 2003
First Named Inventor	Donald E. Steiss
Art Unit	Not Yet Known
Examiner Name	Not Yet Known
Attorney Docket Number	
22347-08261 (Seq. No. 8117)	

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Examiner Initials ¹	Cite No. ¹	Document No.	Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
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Examiner Signature	<i>Jacob Behman</i>	Date Considered	3-22-06
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¹EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609.

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Application No.	10/749,912
Filing Date	December 30, 2003
First Named Inventor	Donald E. Steiss
Art Unit	Not Yet Known
Examiner Name	Not Yet Known

Attorney Docket Number 22347-08261 (Seq. No. 8117)

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OTHER REFERENCES – NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ⁶
J	C1	Boothe, B. and Ranade, A. G., "Improved Multithreading Techniques for Hiding Communication Latency in Multiprocessors," ACM 1992, pp. 214-223.	

Examiner Signature	<i>Jacob Behman</i>	Date Considered	3-22-06
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OTHER REFERENCES – NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
J	C2	Gulati, M. and Bagherzadeh, N., "Performance Study of a Multithreaded Superscalar Microprocessor," 2 nd International Symposium on High-Performance Computer Architecture, February 1996, 11 pages.	
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	C5	Tullsen, D. M. et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proc. Of the 22 nd ISCA, June 1995, 12 pages.	
	C6	Yamamoto, W., "An Analysis of Multistreamed, Superscalar Processor Architectures," Ph.D. Thesis, U.C. Santa Barbara, Dec. 1995, pp. 1-155.	

Examiner Signature	<i>Jacob Petrucci</i>	Date Considered	3-22-06
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